Transformerless Single Phase Inverter Suitable for Grid Connected Application

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Abstract

In Photovoltaic generation system Transformerless inverter has attracted more attention because of its high efficiency output and reduced cost. The transformerless inverter used for grid connected application in which leakage current is one of the main issues this leakage current has to be tackled properly to avoid EMI problem. Hence, the main aim of this paper is how to achieve common mode voltage constant to eliminate the leakage current. This is done by applying any one of the following SPWM strategy it can be: 1. Basic SPWM strategy 2. Bidirectional SPWM control strategy, Thus by applying any one of the strategy mentioned above the leakage current can be reduced by keeping common mode voltage constant, hence by achieving common mode voltage constant high reliability is obtained. By eliminating the dead time effect, low total harmonic distortion is reduced. Because of using three level output voltage the output filter inductance size is reduced this will lead to high efficiency and power density.

1. Introduction

A renewable energy source which is available abundantly in nature, these energies can be used for generation of power easily. The PV generation is one which is used widely all over the world because of its low cost, light weight and economical grid connected inverter which gives high efficiency.

When transformer is connected this provide the galvanic isolation between the grid connection and the PV system. This isolation which avoids the leakage current between the ground and the PV panel, this avoid the system from EMI and system damages problem. To overcome this transformerless grid connected inverter are used. Transformerless grid connected inverter which are developed consequently because of its high power density, high efficiency and low cost. The PV grid connected inverter which is divided into two groups they are

1. With galvanic isolation
2. Without galvanic isolation

Anyone of the following galvanic isolation type can be used

1. High frequency transformer
2. Line frequency transformer

In most of the topologies high frequency transformer is used, it has many power stages it makes the system complex but give high efficiency. The line frequency transformer which makes the system bulky, it reduces the efficiency and system is costly. It is difficult to install the line frequency system. Because of this problems the transformerless inverter are preferred due to its low cost, high efficiency and high power density.

There are many topologies which are used to eliminate the leakage current such as unipolar SPWM, Heric, H5, and H6, The full bridge inverter with unipolar SPWM strategy and bipolar SPWM with full bridge inverter method can be used The proposed inverter topology in this paper has three level output voltage hence a compare to other inverter a smaller filter inductance is used. Because of reduced losses of filter inductor high efficiency is achieved. Therefore two types of unipolar SPWM strategy is used in this paper because of this reliability are increased and there is no dead time needed. Low total harmonic distortion (THD) and unity power factor is achieved.

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2. Proposed Topology

In the anticipated topology circuit, six switches S1, S2, S3, S4, S5 and S6 are used. It has two freewheeling diodes D1 and D2. It is composed of two similar inductor to filter output. The proposed topology uses two SPWM strategies. They are

1. Basic SPWM strategy
2. Bidirectional SPWM strategy

By using the above SPWM strategy the leakage current can be reduced and efficiency is increased.

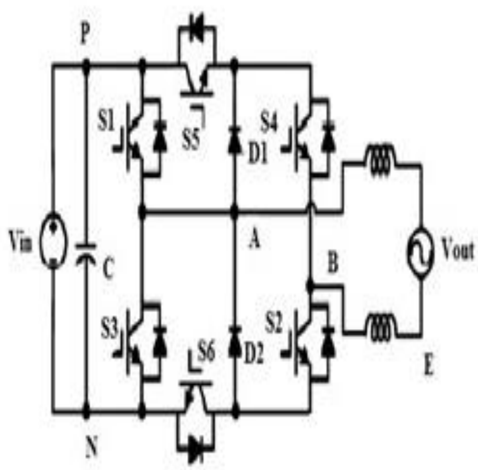

Fig: 1. Proposed Inverter Topology [1]

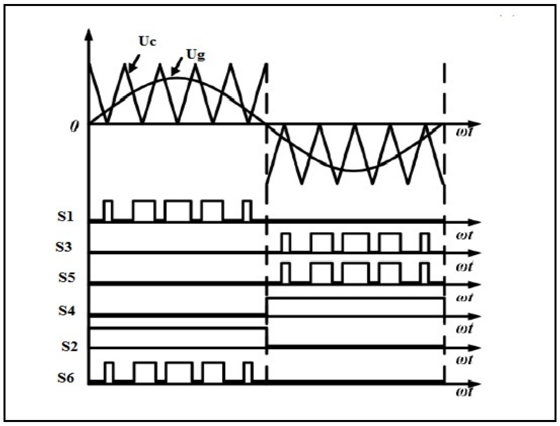

Fig: 2. Basic SPWM Strategy for the proposed inverter [1]

3. Basic SPWM Strategy of Proposed Topology

In the proposed inverter fig 1. Represents the basic SPWM scheme. In the first half cycle i.e., positive half cycle it has two cycles 1. Charging interval 2. Freewheeling interval

During charging time S1, S2, S5 is ON, the current flows through S1, S2, S5. Only S2 is ON during the first positive half cycle, S1 and S5 commutate at high frequency simultaneously [1]. In this condition Van equals +Vin and Vbn equals 0V. Hence Vab equals +V in and the common mode voltage Vcm equals to

$V_{cm} = (V_{an} + V_{bn})/2$

$V_{cm} = (V_{in}+0)/2 = V_{in}/2$ (1)

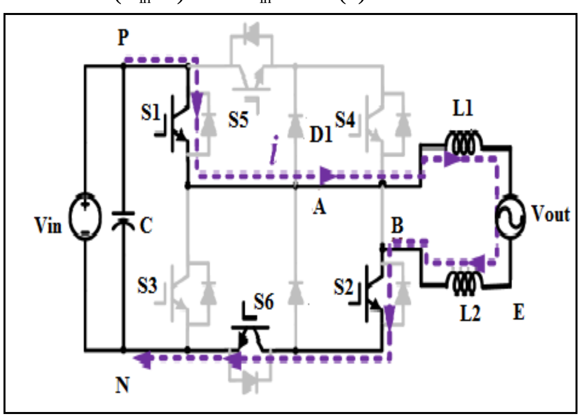

Fig: (3a). Stage 1: Positive half cycle- Charging interval

During the freewheeling interval, switch S2 is ON, the current flows through D2 and S2 which is shown in the fig (3b). In this condition Van falls and Vbn increases, finally they become equal to Vin/2. Hence Vab equals 0V, the common mode voltage equals Vcm;

$$V_{cm} = \frac{Van+Vbn}{2}$$

$$V_{cm} = \frac{Vin/_2 + Vin/_2}{2};$$

$$V_{cm} = \frac{Vin}{2} \quad (2)$$

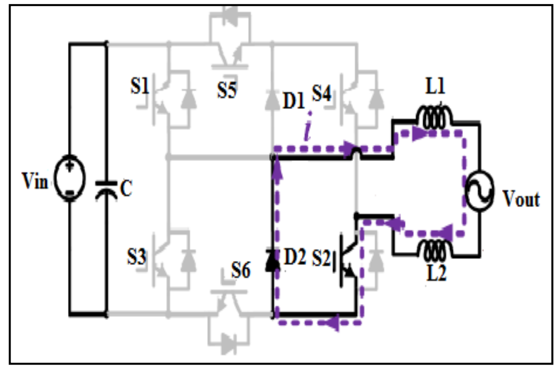

Fig: (3b) Stage 2: Positive half cycle- Freewheeling interval [1]

In the second half cycle i.e., negative half cycle, in this during the charging interval shown in fig (3c) S3, S4 and S6 are ON and Switches S1, S2 and S5 are off in negative half cycle [1]. S4 is always ON, S3and S6 commutate at high frequency.

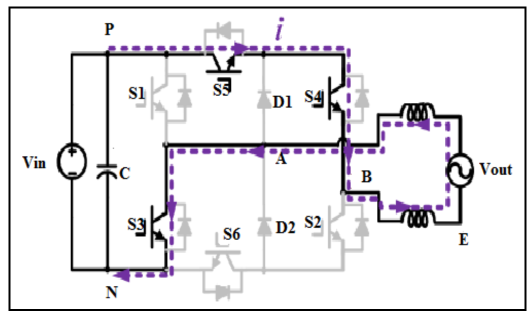

Fig: (3c). Stage 3: Negative half cycle- Charging interval

During the charging interval S2, S4, S6 are ON. The current flows through S2, S4 and S6 [6]. In this condition Van equals 0V, Vbn equals –Vin and common mode voltage Vcm equals to:

$$V_{cm} = \frac{Van+Vbn}{2} = \frac{0+Vin}{2} = \frac{Vin}{2} \quad (3)$$

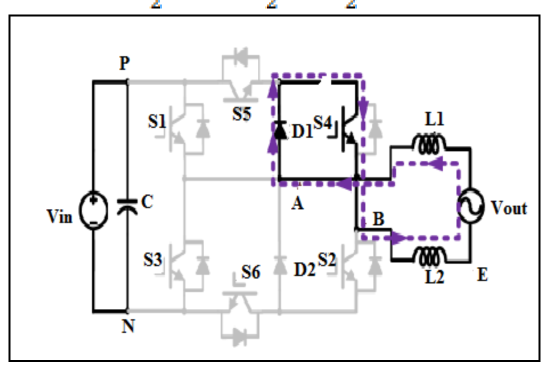

Fig: (3d). Stage 4: Negative half cycle- Freewheeling interval

During the freewheeling interval only switch S4 is ON. The current flows through D2 and S4 [1] as shown in fig (3d). In this condition Van rises and Vbn and Vbn fall until they reach; Vin/2. Hence Vab equals 0V and common mode voltage Vcm equals;

$$V_{cm} = \frac{Van+Vbn}{2}$$

$$V_{cm}=\frac{V_{in}/_2+V_{in}/_2}{2};$$

$$V_{cm}=\frac{V_{in}}{2} \quad (4)$$

Switches S1, S3, S5 and S6 are turned off in the freewheeling interval of both positive and negative half cycle, due to this galvanic isolation is present flanked by the DC side and the grid side. In this condition the common mode voltage Vcm keeps constant in the complete switching period [1]. Therefore three level output voltage is resulted and no leakage current is present in complete system. Switches S2, S4 and S6 are turned OFF in the first positive half cycle hence no dead time is required similarly switches S1, S3 and S5 are turned OFF due to the complete symmetry. Because of no dead time required by means of using the SPWM strategy the current then the reliability of the inverter is improved [1].

Table: 1. Operation of Switch

S1	S2	S3	S4	S5	S6	Van	Vbn	Vcn	
0	0	1	1	1	0	0	$V_{in}/2$	$V_{in}/2$	P
0	0	0	1	0	0	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	
1	1	0	0	0	1	$V_{in}/2$	0	$V_{in}/2$	N
0	1	0	0	0	0	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	

4. Bidirectional SPWM Strategy of Proposed Topology

To attain the high power factor, the grid connected voltage Vgrid and grid connected current Igrid must be kept in phase with each other[1]. The vector diagram of the output of the inverter is shown in the fig 4. Where Vab is the output voltage of the inverter [1] . Vab is derived as;

Vab=Vgrid+jw (L1+L2) Igrid (5)

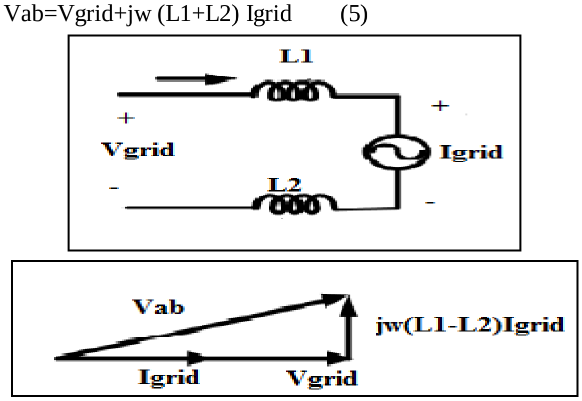

Fig: 4. Vector diagram of inverter output

In the positive half cycle the current Igrid remains negative because of the phase lag [1]. Hence Igrid flows through the anti-parallel diodes of S1, S2 and S5 and inverter operate in stage 5[6]. In this condition Vab equals Vin constantly and no zero voltage is realized [1]. Because of this condition the current in the grid suddenly increases abnormally in the zero crossing intervals which is shown in fig 5.It reduces the grid connected current [1].

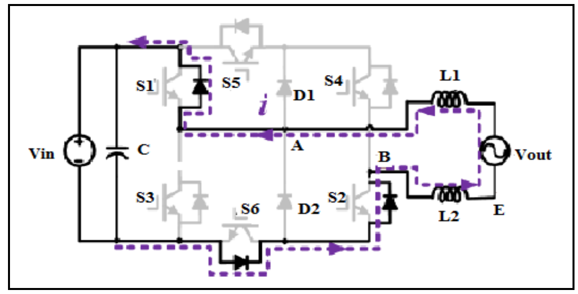

Fig: 5. Zero crossing interval from negative half cycle to positive half cycle [1]

To overcome the above problem the Bidirectional SPWM Strategy is proposed. The below fig6 represents bidirectional SPWM strategy

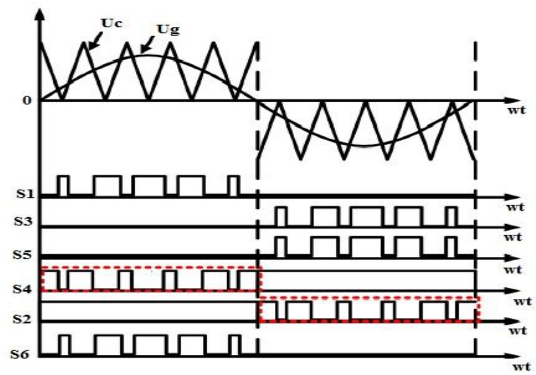

Fig: 6. Bidirectional SPWM Strategy for the proposed inverter

When compared with the basic SPWM strategy the bidirectional SPWM scheme has two differences [1].

1. In positive half cycle S4 is turned ON when S1 is in OFF state
2. In negative half cycle S2 is turned ON when S3 is in OFF state

The inverter operates in both stages (3b) and stage (3d) during the entiregrid period. Zerovoltage can be still implemented to the inverter which improves the grid connected current [1].

In the bidirectional SPWM strategy, dead time is necessary otherwise switches S1,D1,S4,S2,S6 will turn on at the same time in the positive half cycle, which causes the short circuit as shown in below fig 7

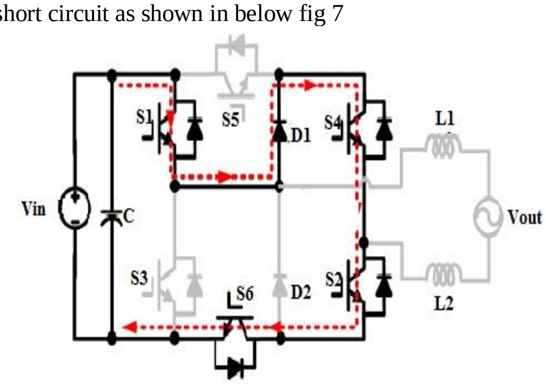

Fig: 7. Short Circuit of Inverter in Bidirectional SPWM Strategy

5. Simulated and Experimental Verification

The parameter of the circuit prototype is given below:
Input DC voltage Vin= 350V
Input DC link capacitance =940µF
Grid Voltage Vgrid=220V
Maximum output power Po=1000w
Output Filter L1=L2= 15mH
Switching Frequency Fs= 16 kHz
PV capacitance C= 10nF

The topology is simulated using MATLAB and the output result is compared between IGBT and MOSFET.

Fig 8 illustrations the simulation results of voltages Van, Vbn and Vab and the common mode voltage Vcm. From this simulation result we can notice that Van and Vbn varies in every PWM cycle. The output voltage Vab is three level due to the unipolar SPWM strategy this helps to decrease the output filter inductance size of the inverter. The parasitic capacitances of photovoltaic array remove the ground leakage current. From the simulation result we can say that common mode voltage Vcm will be kept constant at half of the input DC voltage (175v) [1] in both experimental and simulation result. The THD of Igrid is 0.85% and the PF is 99% even when the THD of Vgrid reaches to 4.26%.

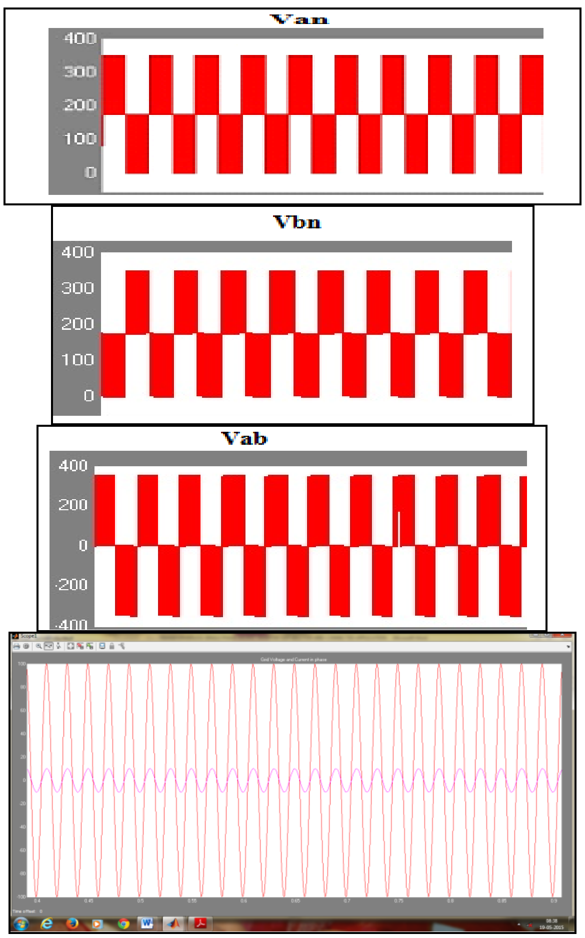

Fig: 8. Simulation Result of Proposed Inverter Topology

6. Conclusion

In the proposed paper the inverter efficiency is increased and high quality grid current is achieved with reduced THD due to using three level voltage output by the SPWM strategy. The dead time effect is greatly reduced in this proposed strategy. The proposed inverter does not produce the leakage current .Lastly the simulated and the experimental results are verified for MOSFET and IGBT. Fromthe simulation we can observe that MOSFET is more effective than the IGBT the THD and Van, Vbn, Vcm is same in both the MOSFET and IGBT. In the experimental MOSFET module is developed where it gives high efficiency because there is no switching losses compared to IGBT. Hence using MOSFET is more advantageous than IGBT this helps in keeping the output high by reducing the THD and keeping efficiency more.

7. Acknowledgement

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